**하드웨어 시스템 설계 6주차 실습 보고서**

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Goal: Implement a simple sequenctial logic (1-sec checker)

Code:

sw2led.v

module sw2led(

input [7:0] SW,

output [7:0] LD

);

assign LD = SW;

endmodule

sw2led.xdc

set\_property PACKAGE\_PIN F22 [get\_ports {SW[0]}];

set\_property PACKAGE\_PIN G22 [get\_ports {SW[1]}];

set\_property PACKAGE\_PIN H22 [get\_ports {SW[2]}];

set\_property PACKAGE\_PIN F21 [get\_ports {SW[3]}];

set\_property PACKAGE\_PIN H19 [get\_ports {SW[4]}];

set\_property PACKAGE\_PIN H18 [get\_ports {SW[5]}];

set\_property PACKAGE\_PIN H17 [get\_ports {SW[6]}];

set\_property PACKAGE\_PIN M15 [get\_ports {SW[7]}];

set\_property IOSTANDARD LVCMOS25 [get\_ports -of\_objects [get\_iobanks 35]];

set\_property PACKAGE\_PIN T22 [get\_ports {LD[0]}];

set\_property PACKAGE\_PIN T21 [get\_ports {LD[1]}];

set\_property PACKAGE\_PIN U22 [get\_ports {LD[2]}];

set\_property PACKAGE\_PIN U21 [get\_ports {LD[3]}];

set\_property PACKAGE\_PIN V22 [get\_ports {LD[4]}];

set\_property PACKAGE\_PIN W22 [get\_ports {LD[5]}];

set\_property PACKAGE\_PIN U19 [get\_ports {LD[6]}];

set\_property PACKAGE\_PIN U14 [get\_ports {LD[7]}];

set\_property IOSTANDARD LVCMOS33 [get\_ports -of\_objects [get\_iobanks 33]];

set\_property IOSTANDARD LVCMOS25 [get\_ports -of\_objects [get\_iobanks 34]];

sec\_checker.v

module sec\_checker(

input gclk,

input rst,

output [7:0] LD

);

reg[26:0] cnt;

reg[7:0] LD\_r;

assign LD = LD\_r;

always @(posedge gclk) begin

if(rst == 1) begin

cnt <= 27'd100000000;

LD\_r <= 0;

end

else if(cnt == 0) begin

cnt <= 27'd100000000;

LD\_r <= LD\_r + 1;

end

else begin

cnt <= cnt - 1;

end

end

endmodule

sec\_checker.xdc

set\_property PACKAGE\_PIN Y9 [get\_ports {gclk}];

set\_property PACKAGE\_PIN P16 [get\_ports {rst}];

set\_property IOSTANDARD LVCMOS33 [get\_ports -of\_objects [get\_iobanks 13]];

set\_property PACKAGE\_PIN T22 [get\_ports {LD[0]}];

set\_property PACKAGE\_PIN T21 [get\_ports {LD[1]}];

set\_property PACKAGE\_PIN U22 [get\_ports {LD[2]}];

set\_property PACKAGE\_PIN U21 [get\_ports {LD[3]}];

set\_property PACKAGE\_PIN V22 [get\_ports {LD[4]}];

set\_property PACKAGE\_PIN W22 [get\_ports {LD[5]}];

set\_property PACKAGE\_PIN U19 [get\_ports {LD[6]}];

set\_property PACKAGE\_PIN U14 [get\_ports {LD[7]}];

set\_property IOSTANDARD LVCMOS33 [get\_ports -of\_objects [get\_iobanks 33]];

set\_property IOSTANDARD LVCMOS25 [get\_ports -of\_objects [get\_iobanks 34]];

Discussion:

gclk = 100MHz, 즉 1초에 1억번 진동하므로 down-counter를 1억으로 설정해주었고, center\_pushbutton을 reset으로 사용하여 down-counter와 up-counter를 리셋하게 구현하였습니다.